

dIgital logic and design

LAB ASESSMENT – 6

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Reg. No: **19BCE0215**

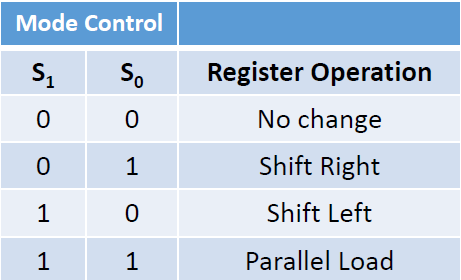
Teacher: **Sairabanu J.**

**Q1) Design Bi-directional shift register.**

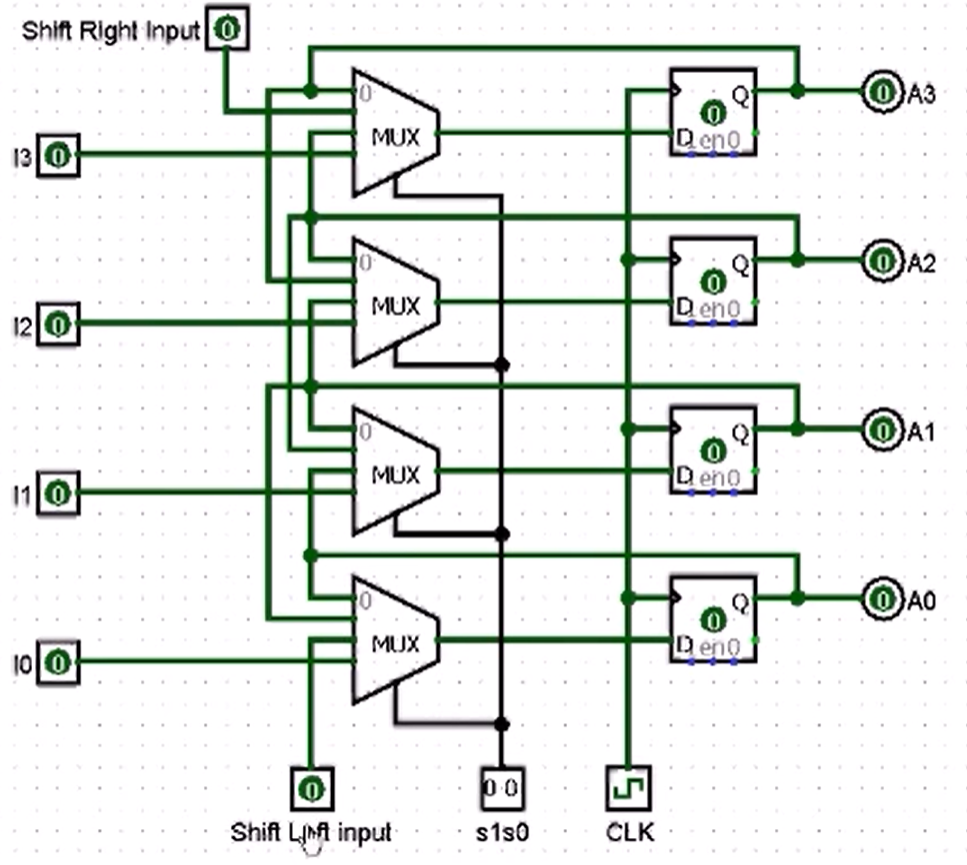
**A1) Design:**

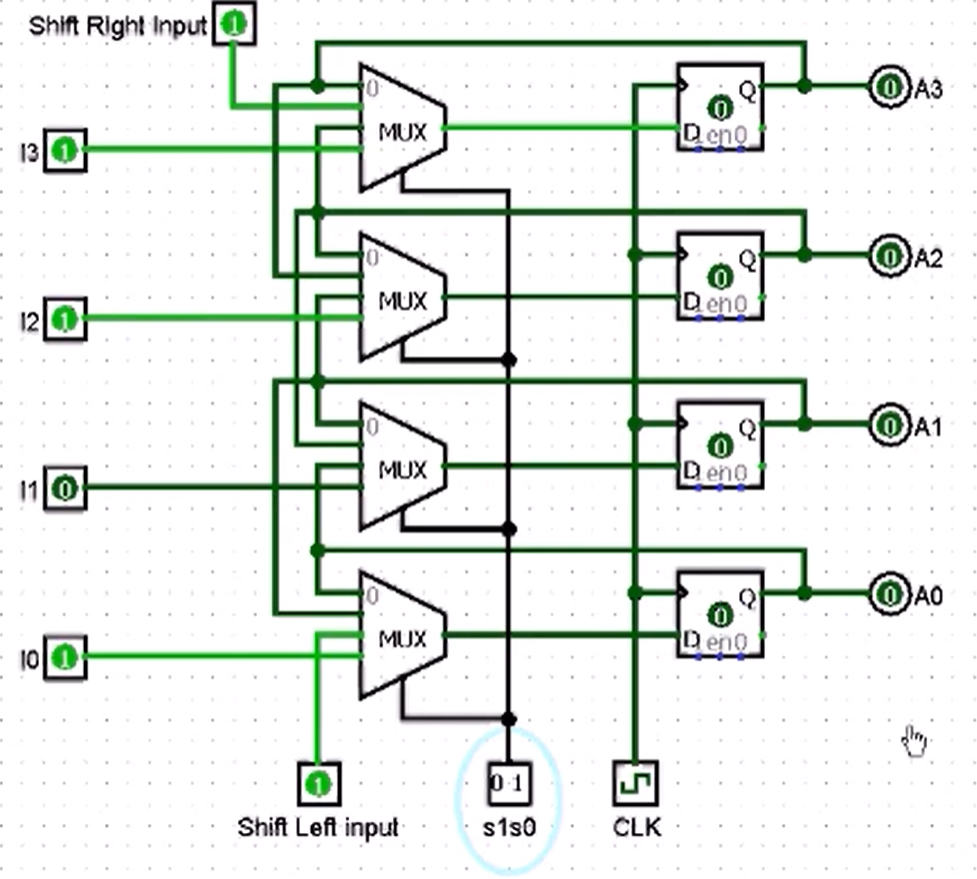
using D flip flops and Multiplexers.

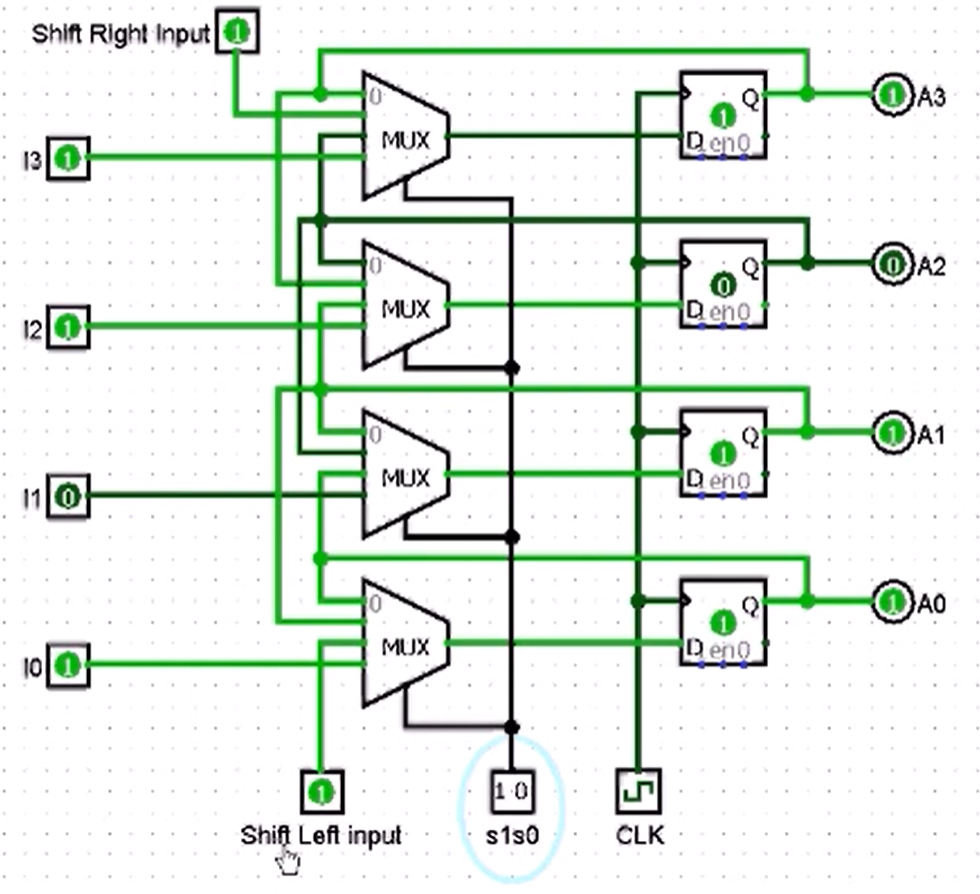
**Truth Table:**

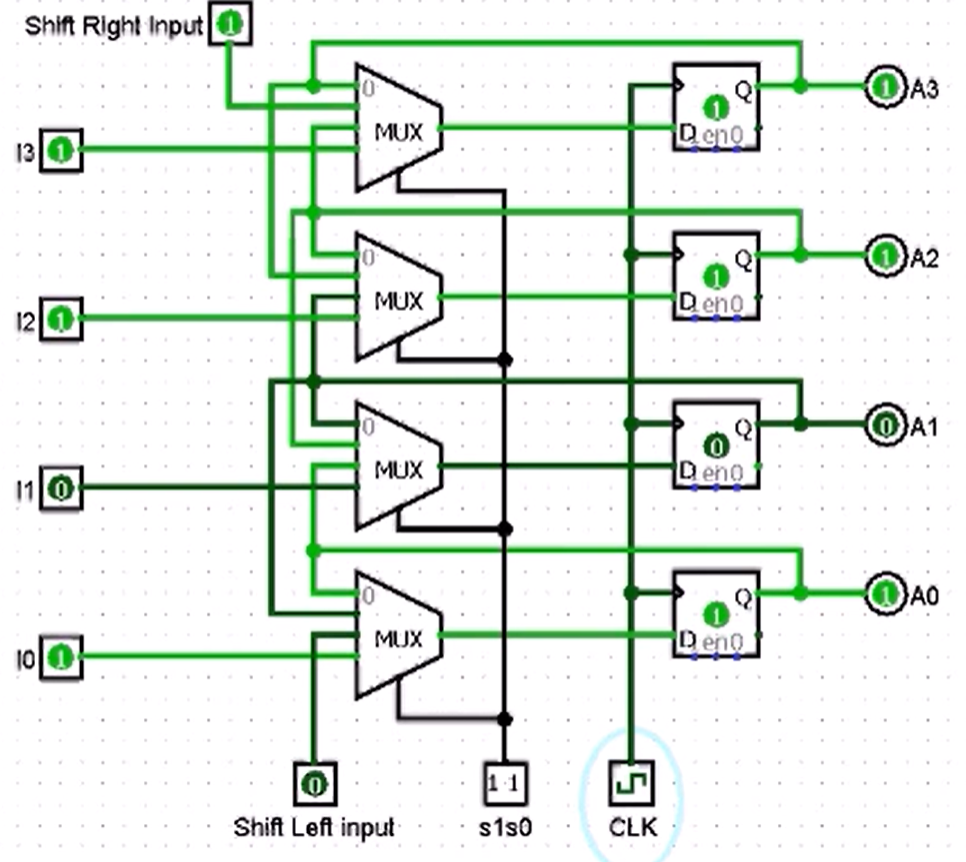


**SCREENSHOTS:**









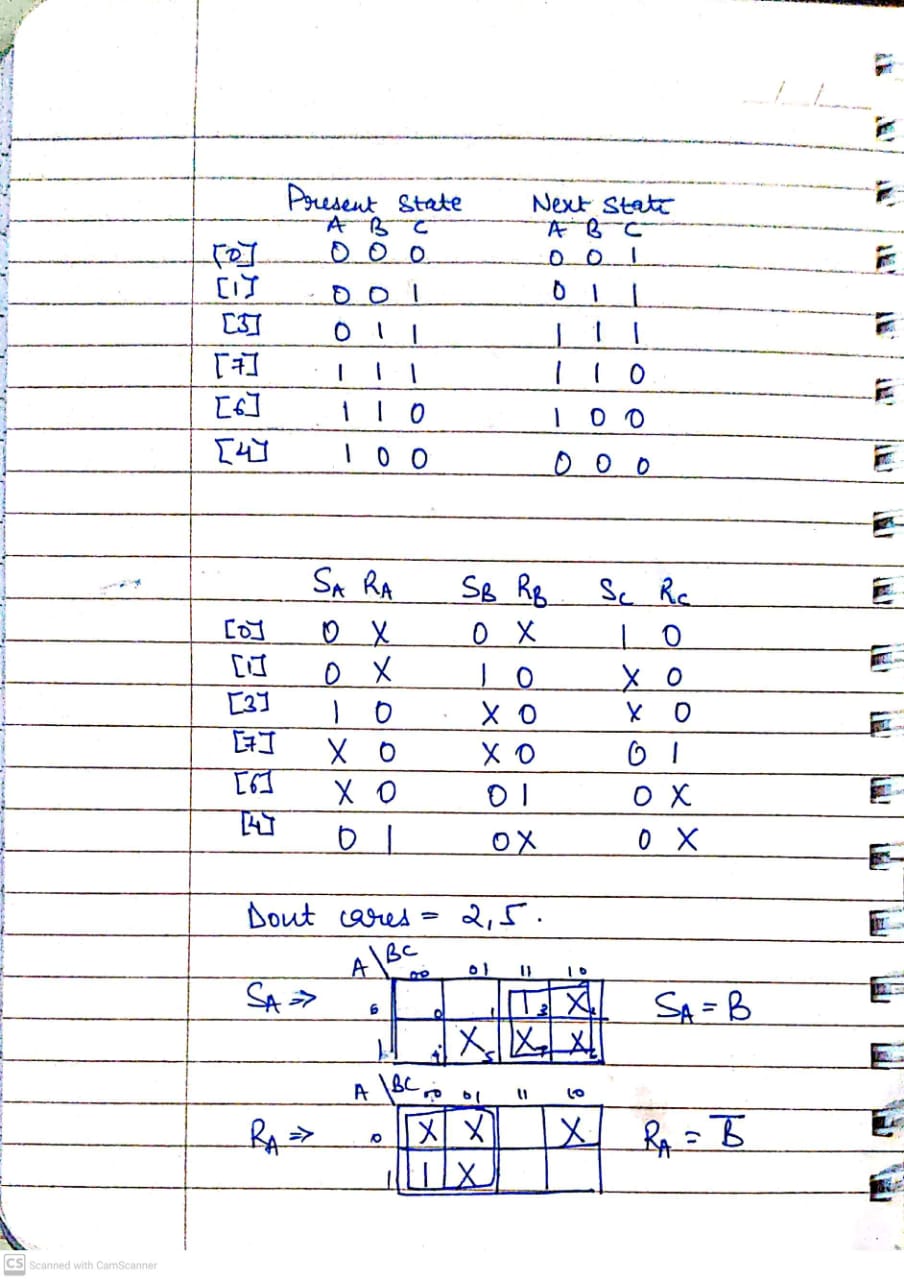
**Q2) To design and implement a binary counter with the repeated sequence as 0, 1, 3, 7, 6, 4 using SR flip flops.**

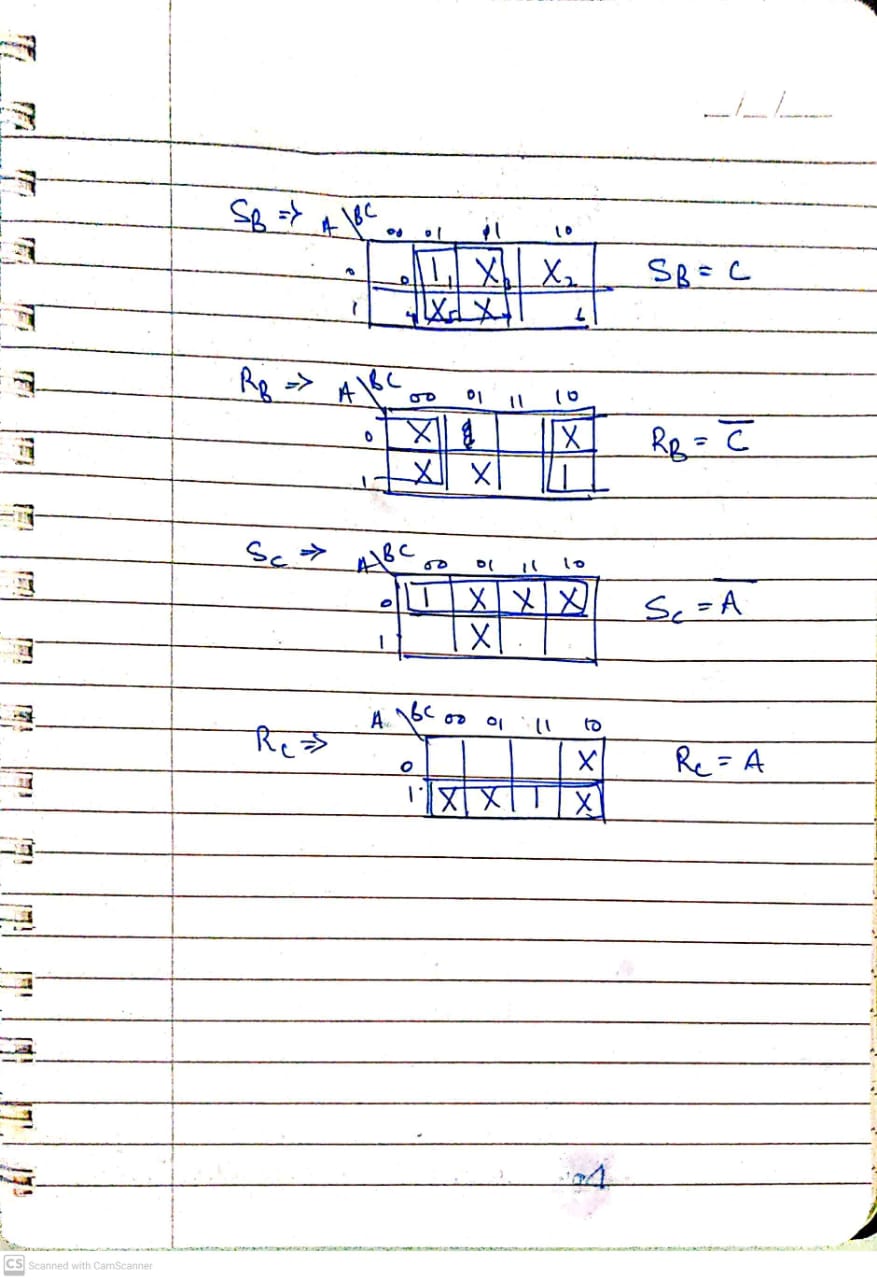
**A2)**

**Design:**

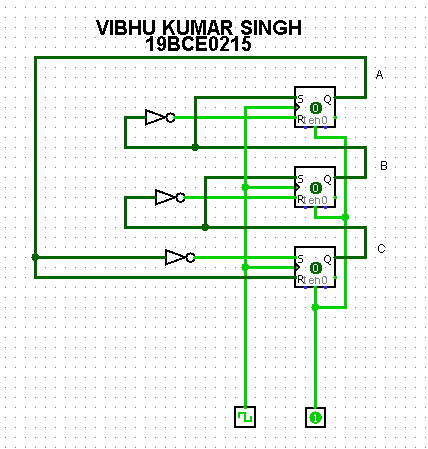
**SR Flip flops are used.**

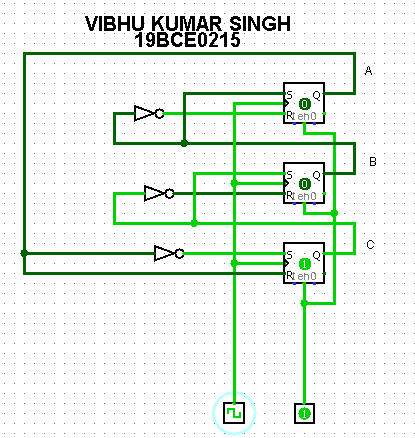
**EQUATIONS:**

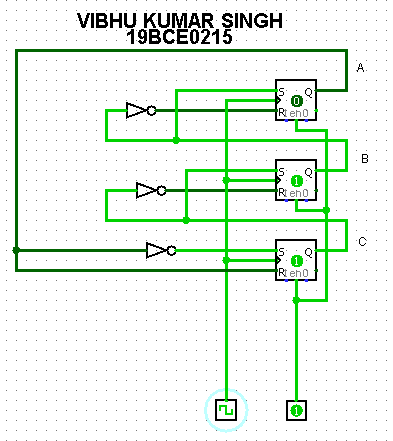


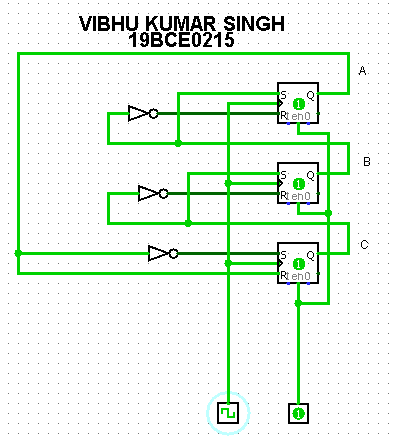


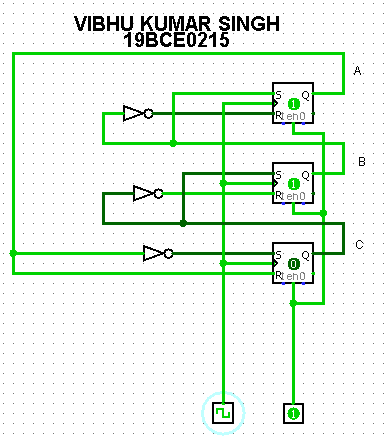
**SCREENSHOTS:**

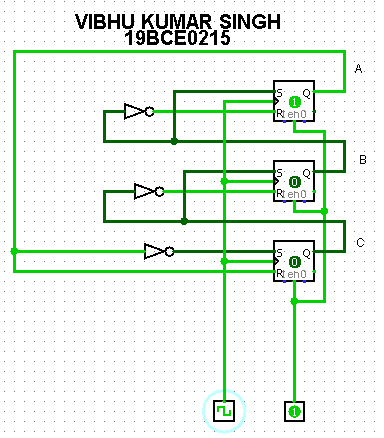










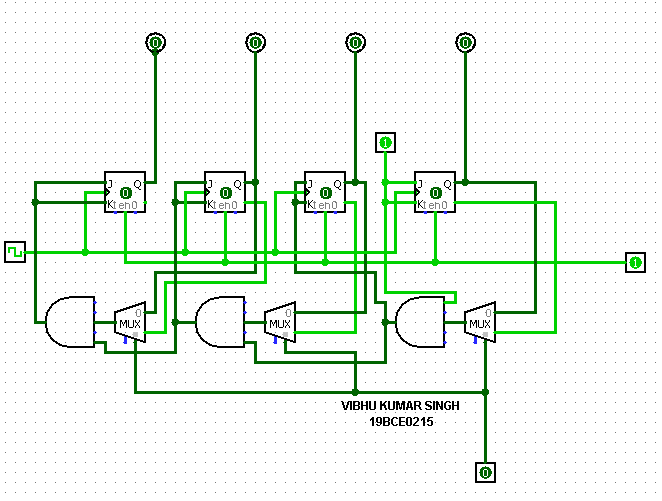


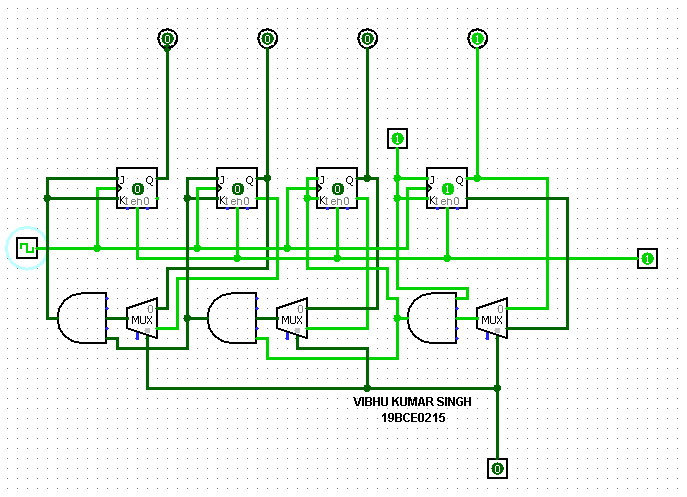
**Q3) To design and implement four bit synchronous up –down binary counter.**

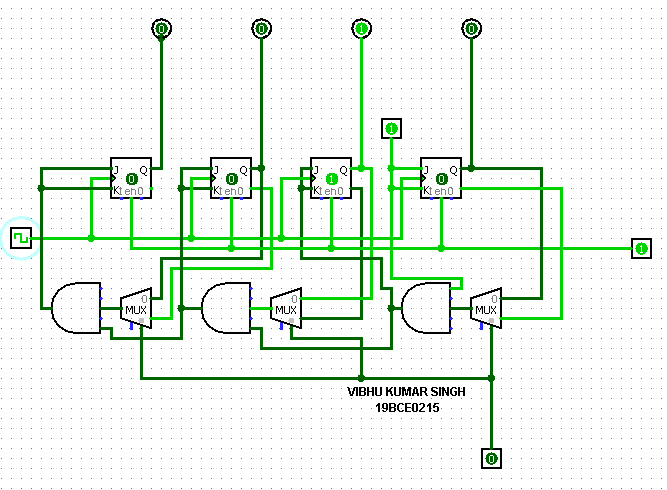
**A3) Design:**

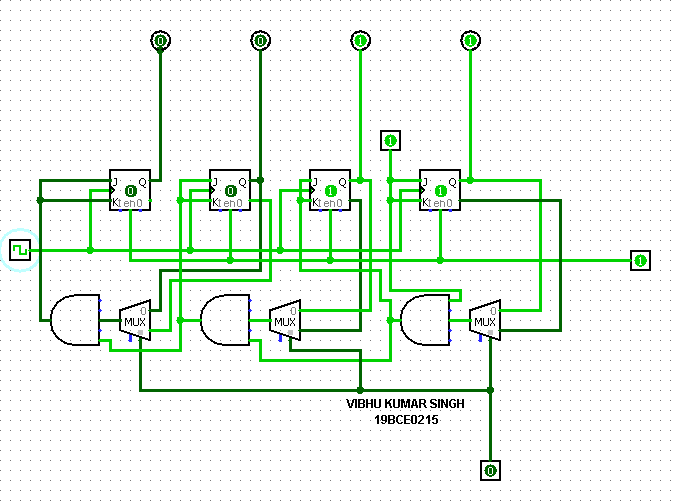
**Using Multiplexer we can do both up and down in the same circuit. When the enable to the MUX is 0, its UP and if it is 1, it is DOWN counter.**

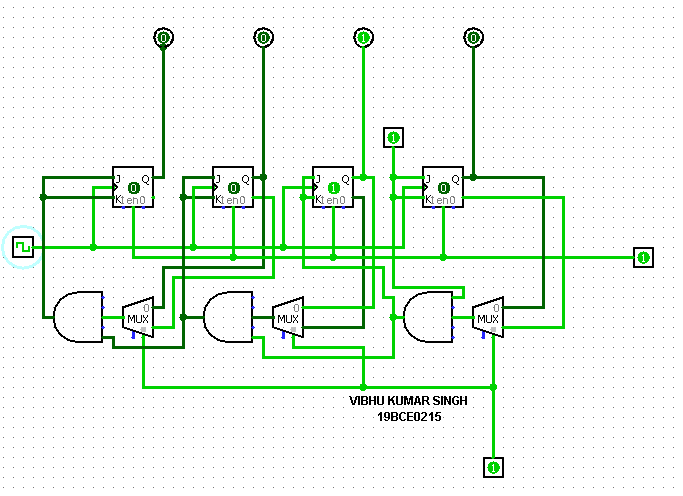
**SCREENSHOTS:**

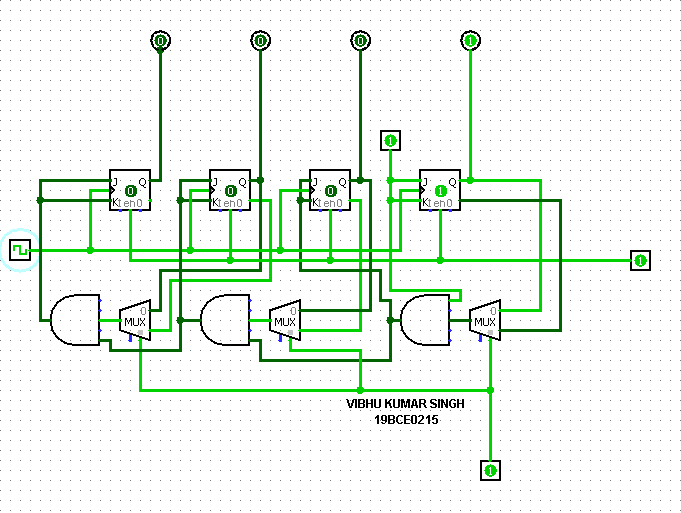


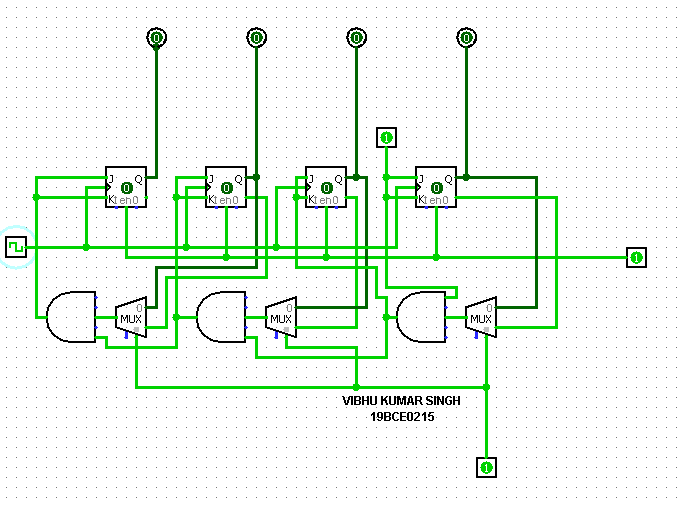










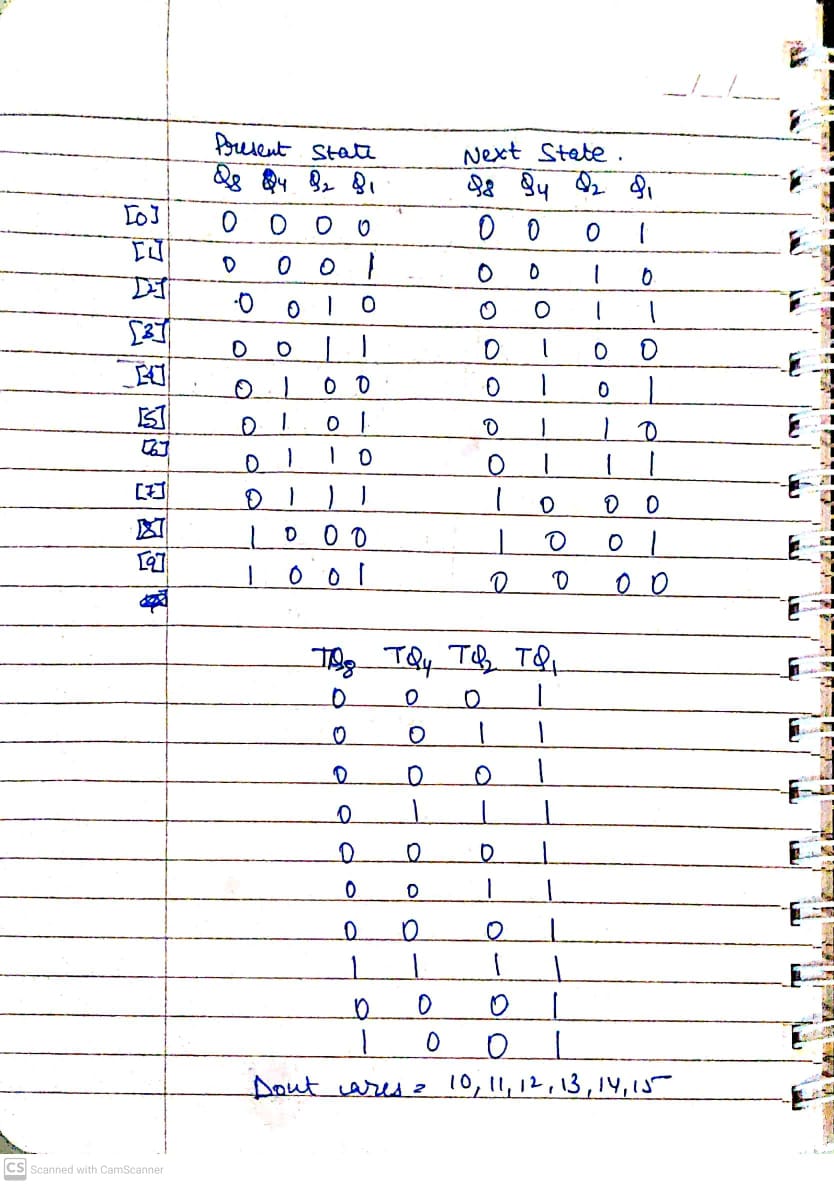


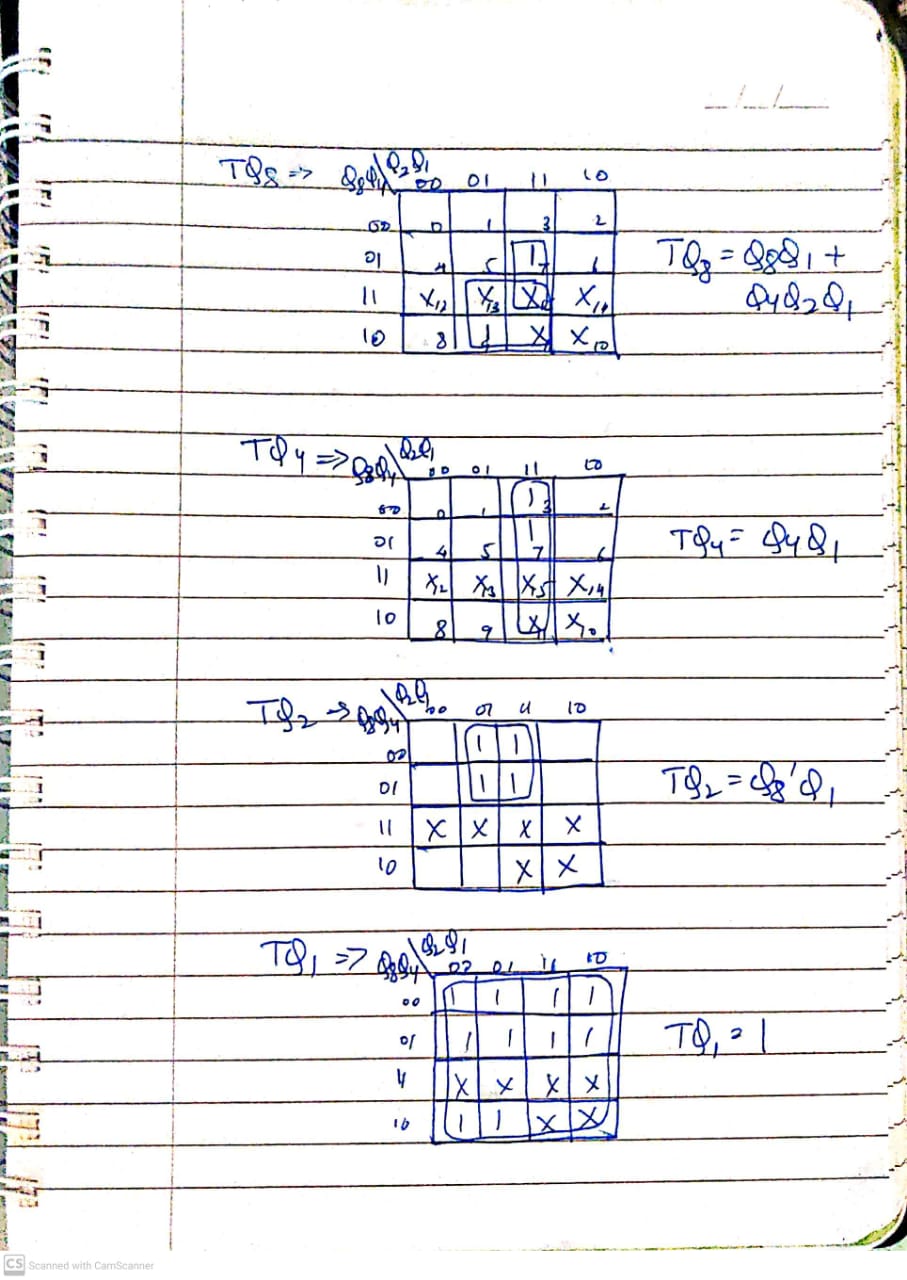
**Q4) To design and implement synchronous BCD counter**

**A4) Design:**

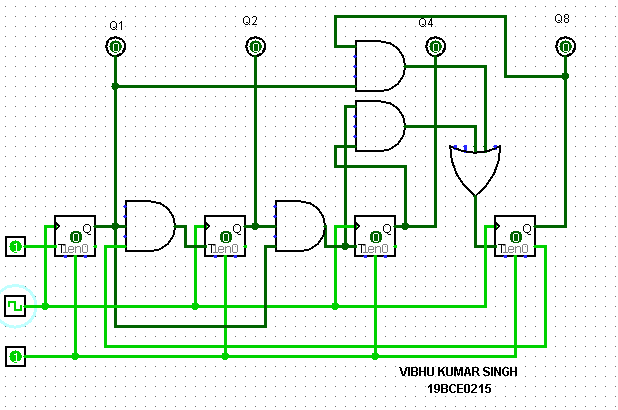
**SR Flip flops are used.**

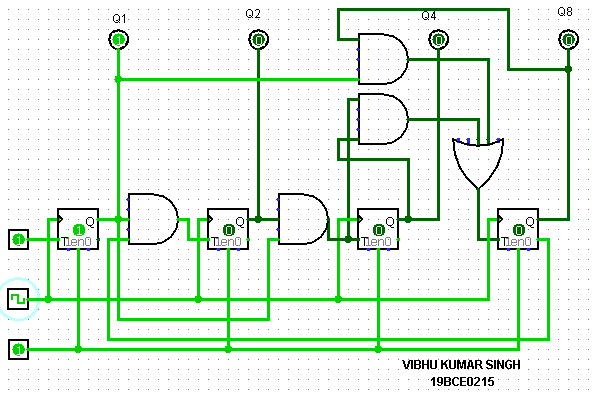
**EQUATIONS:**

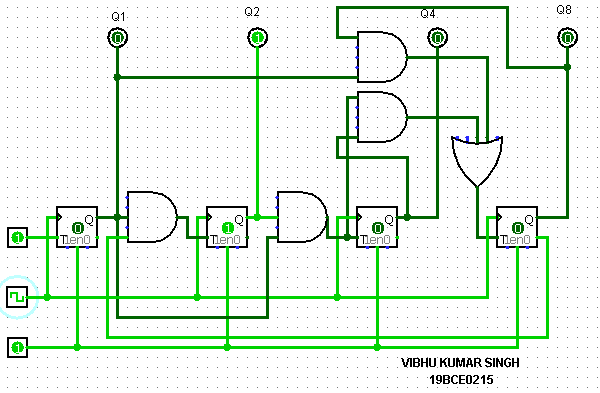


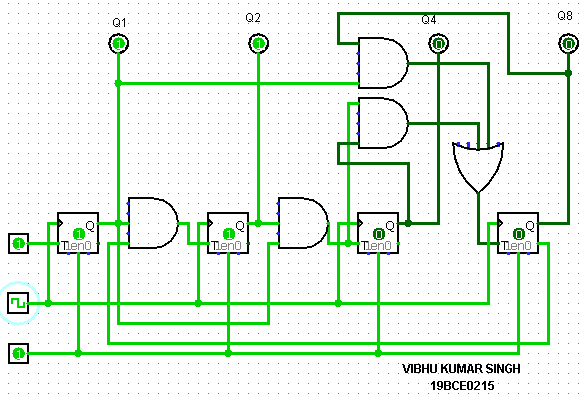


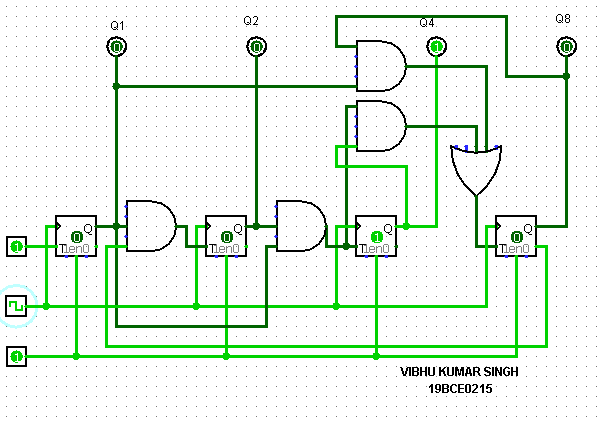
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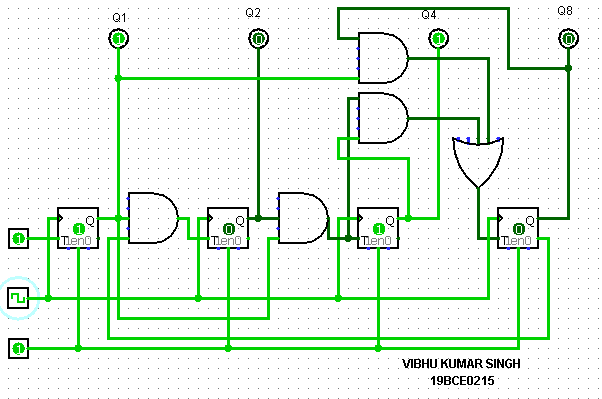
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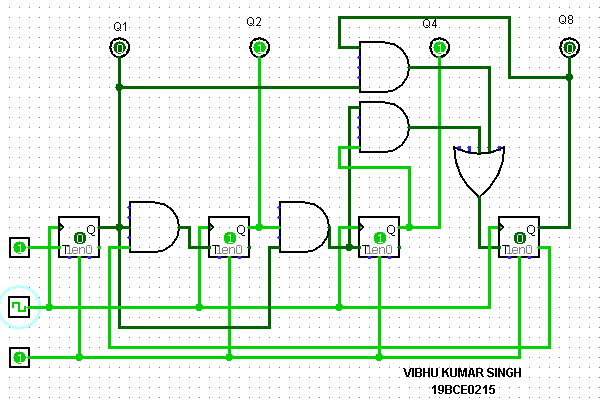
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